US005734843A

United States Patent [19]

Gephardt et al.

[11] Patent Number: 5,734,843

[45] Date of Patent: Mar. 31, 1998

[54] **REVERSE DATA CHANNEL AS A BANDWIDTH MODULATOR**

[75] Inventors: **Douglas D. Gephardt; Brett B. Stewart; Rita M. Wisor; Drew J. Dutton**, all of Austin; **Steven L. Belt**, Pflugerville, all of Tex.

[73] Assignee: **Advanced Micro Devices Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **476,872**

[22] Filed: **Jun. 7, 1995**

[51] **Int. Cl.**[6] **G06F 13/00**

[52] **U.S. Cl.** **395/287**; 395/877

[58] **Field of Search** 395/287, 877; 370/84

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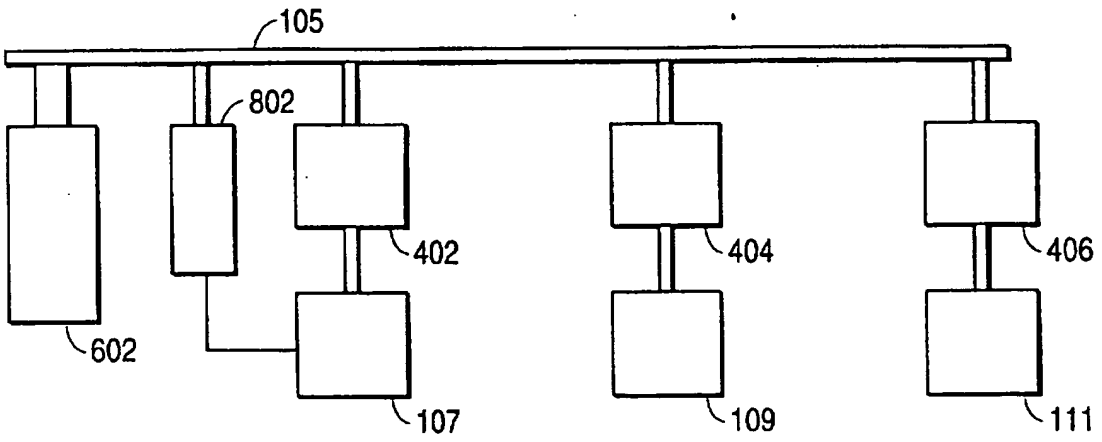
Primary Examiner—Ayaz R. Sheikh

Attorney, Agent, or Firm—Foley & Lardner

[57] **ABSTRACT**

A method of allocating bandwidth among a plurality of devices communicatively connected through a data bus provides for determining a data need of at least one of the plurality of devices, allocating portions of the data bus to the devices in response to the data need, and transmitting data between the devices on the allocated portions of the data bus. The portions of the data bus can be subbusses, each comprising at least one bit line. The data need can be based on a measure of fullness of a buffer corresponding to the at least one device. The data need can be provided as feedback from the buffer to a data bus controller which allocates the portions of the data bus. The method can use rules for assigning the subbusses which are stored in a memory. A processor can change the rules to accommodate changing conditions in the data bus. Also provided is a data communication system comprising a dynamically reconfigurable data bus, a data bus controller connected to the dynamically reconfigurable data bus for configuring subbusses of the data bus, a plurality of receiving devices connected to the data bus, and a feedback connection from at least one of the receiving devices to the data bus controller, wherein the data bus controller configures the subbusses in accordance with feedback received over the feedback connection. A memory can be connected to the data bus controller for storing rules for use by the data bus controller in configuring the subbusses. A processor can change the rules to accommodate changing conditions in the data bus.

9 Claims, 5 Drawing Sheets



to bus **105**. Video feed engine **602** provides the compressed video information to bus **105** which is subsequently received by display devices **107–111**. Video feed engine **602** is also connected to display device **107** via feedback line **604**. This connection allows video feed engine **602** to vary the bandwidth of the data transferred to buffer **402**. For example, video feed engine **602** can vary the number of bit lines in subbus **204**.

In accordance with the invention, video feed engine **602** varies the bandwidth of the data transferred to buffer **402** in accordance with information related to the amount of space available in buffer **402**. For example, if display device **107** reads from buffer **402** a frame comprising a large amount of data, such as frame **1** shown in FIG. **5**, then buffer **402** has vacant space equivalent to the size of frame **1**. On the other hand, if display device **107** reads from buffer **402** a small amount of data, such as frame **2** shown in FIG. **5**, then buffer **402** only has vacant space equivalent to the size of frame **2**.

As display device **107** informs video feed engine **602** of the relative size of the frame or frames most recently read from buffer **402**, video feed engine **602** can adjust the bandwidth of the data transfer to buffer **402**. For example, video feed engine **602** can vary the number of bit lines associated with subbus **204** according to the information received over feedback line **604** from display device **107**. In this way, video feed engine **602** can optimize the bandwidth allocation of bus **105** while minimizing the likelihood of dropped frames due to either condition one or condition two.

Alternatively, instead of display device **107** being connected to video feed engine **602**, buffer **402** can be connected to video feed engine **602** via a feedback line. According to this alternative configuration, buffer **402** would provide similar information to video feed engine **602** as that supplied by display device **107** in the embodiment described above. Thus, as it provides a frame to display device **107**, buffer **402** can inform video feed engine **602** of the size of the frame so that video feed engine **602** can adjust the bandwidth to buffer **402** accordingly.

Similarly, in addition to display device **107** providing feedback to video feed engine **602** over feedback line **604**, display devices **109** and **111** can also provide feedback to video feed engine **602** over feedback lines connected between these devices and video feed engine **602** in a manner similar to the feedback provided by display device **107**. Thus, video feed engine **602** can optimize the bandwidths to each of the buffers **402–406** based on feedback from each of the display devices.

To arbitrate likely contests between the devices for the bandwidth of data bus **105**, video feed engine **602** can conduct tradeoff analyses to determine the optimal bandwidths to be allocated to each of the devices based on the respective data needs of the devices. These tradeoff analyses can be performed in accordance with rules stored in a memory, such as memory **701** shown in FIG. **7**. Further, the rules for conducting these tradeoff analyses can be changed by a processor such as processor **703**.

As discussed earlier with respect to buffer **402**, buffers **404** and **406** can similarly provide feedback to video feed engine **602** in the alternative embodiment. Video feed engine **602** then conducts tradeoffs in a manner similar to that discussed above for the embodiment with feedback from the multiple display devices.

Alternatively, as shown in FIG. **8**, feedback from a device such as display device **107** can be provided to data bus controller **802**. In this embodiment, data bus controller **802** controls the bandwidth of the portion of data bus **105** that is associated with buffer **402** in accordance with the feedback received from display device **107**. Similarly, devices **109** and **111** can provide feedback to data bus controller **802**. Alternatively, one or more of buffers **402–406** could provide feedback to data bus controller **802**. Data bus controller **802** can then reconfigure data bus **105** by, for example, reconfiguring the subbusses associated with the display devices and buffers according to the feedback.

In a manner similar to that described earlier, data bus controller **802** can be connected to a memory such as memory **701** shown in FIG. **7** in order to conduct tradeoff analyses in accordance with rules contained in the memory. Similarly, a processor such as processor **703** can change the rules contained in the memory to accommodate changing conditions of the data bus.

While several embodiments of the invention have been described, it will be understood that it is capable of further modifications, and this application is intended to cover any variations, uses, or adaptations of the invention, following in general the principles of the invention and including such departures from the present disclosure as to come within knowledge or customary practice in the art to which the invention pertains, and as may be applied to the essential features hereinbefore set forth and falling within the scope of the invention or the limits of the appended claims.

What is claimed is:

1. A method of allocating bandwidth among a plurality of devices communicatively connected through a data bus, the method comprising the steps of:

determining an availability of data storage space associated with at least one of the plurality of devices;

allocating portions of the data bus to the devices in response to said data storage space availability associated with said at least one device; and

transmitting data between the devices on the allocated portions of the data bus;

wherein said data storage space availability is based on a measure of fullness of a buffer corresponding to the at least one device; and

wherein said data storage space availability is provided as feedback from the buffer to a data bus controller which allocates the portions of the data bus.

2. The method recited in claim **1**, wherein said portions of the data bus are subbusses, each comprising at least one bit line.

3. A method of allocating subbusses among a plurality of receiving devices communicatively connected to a data bus, the method comprising the steps of:

determining an availability of data storage space of at least one of the plurality of receiving devices based on an amount of data storage space available in a corresponding buffer;

feeding back a feedback signal indicating said amount of data storage space available to a bus controller;

allocating subbusses of the data bus to the receiving devices in response to said feedback signal; and

transmitting data between the devices on the allocated subbusses.

4. The method recited in claim **3**, further comprising using arbitration rules for assigning said subbusses.

5. The method recited in claim **4**, wherein a processor changes said rules to accommodate changing conditions in the data bus.

6. A data communication system comprising:

a dynamically reconfigurable data bus;

39/3,K/24 (Item 24 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015403631 **Image available**
WPI Acc No: 2003-465771/200344
XRPX Acc No: N03-370455
Configurable bus allocation **method in multiprocessor data processing system, involves** allocating **buses of processor chip to external** components **based on** bus allocation **priority determined according maximum use of** bus **bandwidth**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: ARIMILLI L B; ARIMILLI R K; CLARK L J; FIELDS J S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6535939	B1	20030318	US 99436418	A	19991109	200344	B

Priority Applications (No Type Date): US 99436418 A 19991109
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6535939	B1		14	G06F-013/14	

Configurable bus allocation **method in multiprocessor data processing system, involves** allocating **buses of processor chip to external** components **based on** bus allocation **priority determined according maximum use of** bus **bandwidth**

Abstract (Basic):
... Priority of **allocation** for configurable buses of a processor chip to external **components** coupled to the chip, is determined based on the maximum use of the **bus** bandwidth. The configurable buses are dynamically **allocated** to the external **components** , based on the priority using software manipulation of a **bus allocation** unit of the processor chip.
... 1) configurable **bus allocation** system; and...

...For **allocating** configurable buses of processor chip to external **components** such as memory in **symmetric** multiprocessors (SMP) data processing system...

...Since the priority is calculated based on the maximum efficient use of processor's **bus** bandwidth, faster processing is enabled within the data processing system. Hence, overall efficiency of the...

...The figure shows a flowchart explaining the configurable **bus allocation** process...
...Title Terms: **BUS** ;
International Patent Class (Main): **G06F-013/14**
Manual Codes (EPI/S-X): **T01-H07A** ...

... **T01-H07C7** ...

... **T01-M02C1**

US006535939B1

(12) **United States Patent**
Arimilli et al.

(10) **Patent No.: US 6,535,939 B1**
(45) **Date of Patent: Mar. 18, 2003**

(54) **DYNAMICALLY CONFIGURABLE MEMORY BUS AND SCALABILITY PORTS VIA HARDWARE MONITORED BUS UTILIZATIONS**

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(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/436,418**

(22) Filed: **Nov. 9, 1999**

(51) **Int. Cl.**[7] **G06F 13/14**
(52) **U.S. Cl.** **710/116**; 710/305
(58) **Field of Search** 710/110, 107, 710/113, 116, 123, 33, 36, 41, 300, 305, 309, 311

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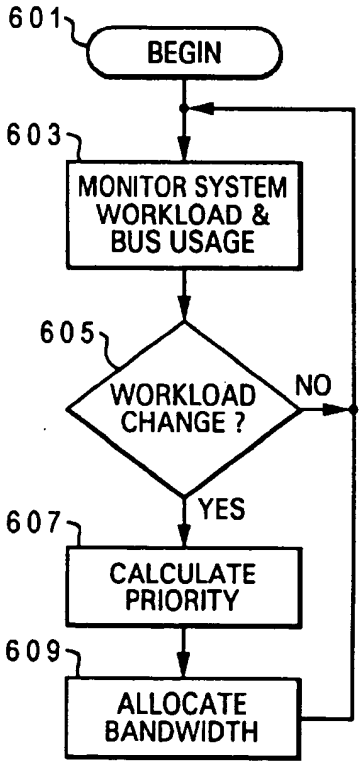
Primary Examiner—Glenn A. Auve

(57) **ABSTRACT**

A data processing system with configurable processor chip buses. The processor chip is designed with a bus allocation unit and has a plurality of extended buses of which a number are configurable buses (i.e. may be dynamically allocated to any one of several external components, particularly memory and other SMPs). A priority determination of bandwidth requirements of the external components is made during system processing. Then the configurable buses are dynamically allocated to the external components based on their bandwidth requirement and/or the configuration which provides the best overall system efficiency.

21 Claims, 5 Drawing Sheets



required bandwidth) (step **605**). When a workload change is detected (i.e. more memory data bandwidth requested or more processing power bandwidth requested), the logic within the switch topology calculates a priority of the various external components (step **607**). Finally, the switch system allocates the available configurable buses (step **609**) based on the results of the priority determination. In the preferred embodiment, the priority determination calculates based on the most efficient use of the processor's bus bandwidth, thus resulting in faster processing within the system.

In one embodiment, the process includes the steps of determining whether the allocation measure is static or dynamic. In another embodiment, the process further includes determining whether the logic within the switch topology is being controlled by the software instructions or the hardware bus allocation logic/unit. In other embodiments, the steps further include determining the number of buses which are allocatable (i.e., configurable) and which number to allocate to which external components. It is expected that in a multi-scalable bus allocation configuration, that some of the configurable buses are allocated to one external component, while the other configurable buses are allocated to another external component.

As a final matter, it is important that while an illustrative embodiment of the present invention has been, and will continue to be, described in the context of a fully functional data processing system, those skilled in the art will appreciate that the software aspects of an illustrative embodiment of the present invention are capable of being distributed as a program product in a variety of forms, and that an illustrative embodiment of the present invention applies equally regardless of the particular type of signal bearing media used to actually carry out the distribution. Examples of signal bearing media include recordable type media such as floppy disks, hard disk drives, CD ROMs, and transmission type media such as digital and analogue communication links.

While an illustrative embodiment has been particularly shown and described, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the illustrative embodiment. Most notably, although the invention has been described with reference to memory and other SMPs as the external components, the invention can be implemented with other external components, such as the I/O and lower level caches. Further, there is no requirement that the other processors be SMP processors. Those skilled in the art can appreciate that other multi-processor configurations may be utilized in the implementation of the invention.

What is claimed is:

1. A method for allocating configurable buses of a processor chip to external components coupled to said processor chip, said method comprising the steps of:

determining a priority of allocation for one or more configurable buses of a processor chip to each of said external components coupled to said processor chip to substantially maximize efficient use of said one or more configurable buses; and

dynamically allocating said one or more configurable buses to said external components based on said priority utilizing software manipulation of a bus allocation unit of said processor chip.

2. The method of claim **1**, wherein said determining step is controlled by a software code and includes the steps of:

configuring an Instruction Set Architecture (ISA) with an allocation bit, which controls said bus allocation unit;

calculating said priority during compilation of instructions of a software program; and

encoding a priority value in said allocation bit of instructions of the software program.

3. The method of claim **1**, wherein:

said determining step includes the step of prioritizing said each of said external components which utilize said configurable buses; and

said allocating step includes the steps of:

increasing an allocation of buses to an external component having a highest priority; and

simultaneously decreasing an allocation of buses to another external component with a lower priority.

4. The method of claim **3**, wherein said allocating step allocates a single configurable bus as an additional bus to an external component having a highest priority.

5. The method of claim **3**, wherein when there are more than one configurable buses that can be allocated, said allocating step includes:

dividing said more than one configurable buses into subsets for allocation to different components requiring use of bus bandwidth, each of said subset having zero or more configurable buses and a sum of said subsets equaling a total number of configurable buses;

allocating a first subset of buses to a first component having a first priority and a second subset of buses to a second component having a second priority, such that the number of buses in the first subset and second subset are proportional to the amount of bus bandwidth required for said first and second components, respectively.

6. The method of claim **1**, wherein said bus allocation unit includes a mode register, said dynamically allocating step further includes the step of setting the mode register to reflect the allocation scheme utilized by the buses.

7. A method for allocating configurable buses of a processor chip to external components coupled to said processor chip, said method comprising the steps of:

determining a priority of allocation for one or more configurable buses of a processor chip to each of said external components coupled to said processor chip to substantially maximize efficient use of said one or more configurable buses, wherein said determining step is workload dependent; and

dynamically allocating said one or more configurable buses to said external components based on said priority utilizing software manipulation of a bus allocation unit of said processor chip, said dynamically allocating step allocates said configurable bus to said external component via a switch and includes:

terminating all buses of said processor chip and buses of said external components at a switch, said switch having associated switch logic; and

instantiating said allocation of configurable buses of said processor chip utilizing said associated switch logic.

8. A system for allocating configurable buses of a processor chip to external components of a data processing system, said system comprising:

means for determining a priority of allocation for one or more configurable buses of a processor chip to each of said external components coupled to said processor chip to substantially maximize efficient use of said configurable buses; and

39/3,K/66 (Item 66 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012029757 **Image available**
WPI Acc No: 1998-446667/199838
Related WPI Acc No: 1998-018715; 1998-250848; 1998-311843; 1998-311845; 1999-166911; 1999-478179; 1999-570483; 2000-269609; 2000-302753; 2000-375415
XRPX Acc No: N98-348228

Computer system with centralised input-output processor used in multimedia application - comprises input-output processor connected **with multimedia** bus **by which data** allocation **to multimedia** devices **from** bus **is controlled based on stored data transfer rate**

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: BELT S L; SWANSTROM S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5790815	A	19980804	US 95559661	A	19951120	199838 B
			US 96650939	A	19960517	

Priority Applications (No Type Date): US 95559661 A 19951120; US 96650939 A 19960517
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5790815	A		43	G06F-013/38	Cont of application US 95559661

... **comprises input-output processor** connected **with multimedia** bus **by which data** allocation **to multimedia** devices **from** bus **is controlled based on stored data transfer rate**

...Abstract (Basic): The system comprises a bridge logic unit (106) which is **connected** between a CPU (102) and a main memory (110). The bridge logic unit comprises a...

...the main memory is controlled to store the processed data from the CPU. An expansion **bus** (120) is **connected** with the bridge logic through an expansion **bus interface** of the bridge logic. A multimedia **bus** (130) is **coupled** with the bridge logic by which the data stream is **divided** into multiple data bytes...

...Multiple multimedia **devices** (142,144,146) are **coupled** with the multimedia **bus** through the multimedia **bus interface** logic by which the multimedia **bus** is accessed by the multimedia **devices** for data communication. A centralised input-output processor (702) is **connected** with the multimedia **bus** , in which the data transmission rate, data source and data destination information are stored. Based on the stored information, the multimedia **bus** access by the multimedia **device** is controlled **dynamically** and selectively...'

...ADVANTAGE - Improves performance characteristic and data throughput using **PCI** data line and multimedia **bus** . Enables time slot **allocation dynamically corresponding** to received bandwidth. Enables **distributed** and centralised processor improvement on multimedia **bus** .

...Title Terms: **CONNECT** ;

International Patent Class (Main): **G06F-013/38**
Manual Codes (EPI/S-X): **T01-C07C5** ...

... **T01-H07A1** ...

... **T01-J30**

US005790815A

United States Patent [19]

Swanstrom et al.

[11] Patent Number: 5,790,815

[45] Date of Patent: Aug. 4, 1998

[54] **COMPUTER SYSTEM HAVING A MULTIMEDIA BUS AND COMPRISING A CENTRALIZED I/O PROCESSOR WHICH PERFORMS INTELLIGENT BYTE SLICING**

[75] Inventors: **Scott Swanstrom**, Austin; **Steven L. Belt**, Pflugerville, both of Tex.

[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **650,939**

[22] Filed: **May 17, 1996**

Related U.S. Application Data

[63] Continuation of Ser. No. 559,661, Nov. 20, 1995.

[51] **Int. Cl.**[6] **G06F 13/38**

[52] **U.S. Cl.** **395/309**; 395/306; 395/308

[58] **Field of Search** 395/650, 308, 395/309, 728, 729, 293, 847

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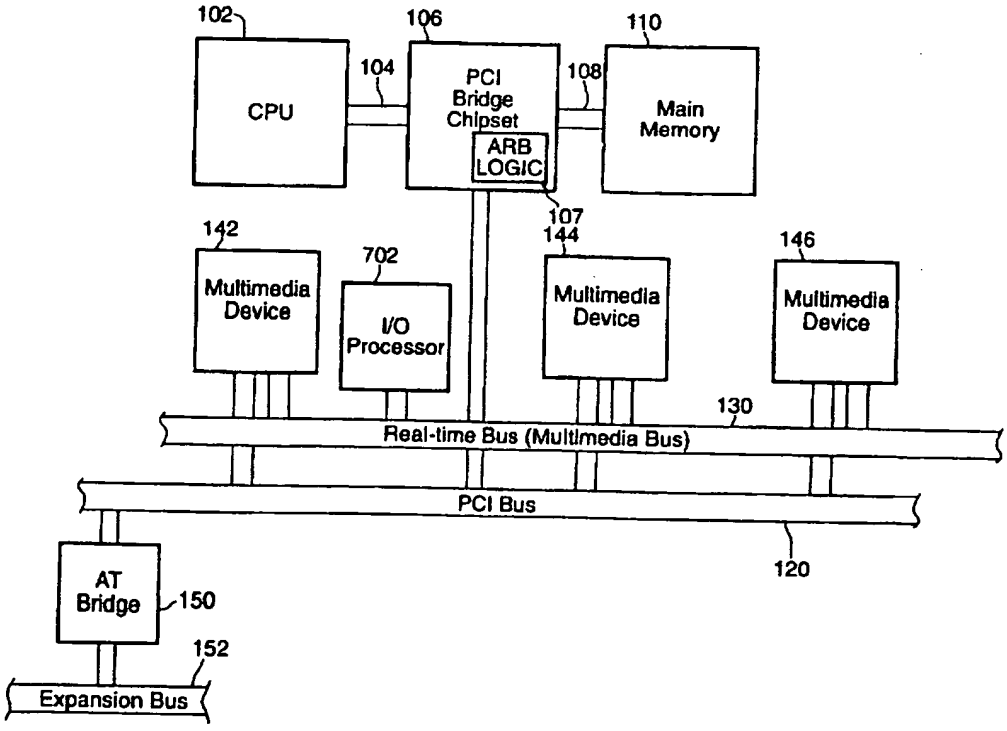
Primary Examiner—Jack B. Harvey
Assistant Examiner—Jigar Pancholi
Attorney, Agent, or Firm—Conley, Rose & Tayon; Jeffrey C. Hood

[57] **ABSTRACT**

A computer system optimized for real-time applications which provides increased performance over current computer architectures. The system includes a standard local system bus or expansion bus, such as the PCI bus, and also includes a dedicated real-time bus or multimedia bus. Various multimedia devices are coupled to one or more of the expansion bus and/or the multimedia bus. The computer system includes byte slicing logic coupled to one or more of the expansion bus and/or the multimedia bus which operates to allow different data streams to use different byte channels simultaneously. Thus the byte sliced multimedia bus allows different peripherals to share the bus simultaneously. The byte slicing logic thus may assign one data stream to a subset of the total byte lanes on the multimedia bus, and fill the unused byte lanes with another data stream. The computer system of the present invention thus provides much greater performance for real-time applications than prior systems.

15 Claims, 26 Drawing Sheets



39/3,K/30 (Item 30 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014834115 **Image available**
WPI Acc No: 2002-654821/200270
XRPX Acc No: N02-517354
Bus **arbitration system for computer system** allocates **timeslots for** bus **service duration on** bus **for** peripheral device **based on request signals, by issuing grant signal to** peripheral device
Patent Assignee: LUCENT TECHNOLOGIES INC (LUCE)
Inventor: PRASANNA G N I
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6425032	B1	20020723	US 99292397	A	19990415	200270	B

Priority Applications (No Type Date): US 99292397 A 19990415
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6425032	B1		14	G06F-013/362	

Bus **arbitration system for computer system** allocates **timeslots for** bus **service duration on** bus **for** peripheral device **based on request signals, by issuing grant signal to** peripheral device
Abstract (Basic):
... A **peripheral device** transmits periodic and aperiodic request signals to a processor. The processor **dynamically allocates** time slots for a **bus** service duration on **bus** for the **peripheral device** based on the request signals, by issuing a grant signal to **peripheral device** . A memory (190) **connected** to the processor, stores the information related to the request signals and the associated grant...
... 2) Time **allocation** method...

...Minimizes queue length and reduces the data delay experienced at each **peripheral device** by **dynamically allocating** time slots on data **bus** .

Title Terms: **BUS** ;
International Patent Class (Main): **G06F-013/362**
Manual Codes (EPI/S-X): **T01-G05C1** ...

... **T01-H05B3** ...

... **T01-H07A2**

US006425032B1

(12) **United States Patent**
Prasanna

(10) **Patent No.: US 6,425,032 B1**
(45) **Date of Patent: Jul. 23, 2002**

(54) **BUS CONTROLLER HANDLING A DYNAMICALLY CHANGING MIX OF MULTIPLE NONPRE-EMPTABLE PERIODIC AND APERIODIC DEVICES**

(75) Inventor: **G. N. Srinivasa Prasanna**, Bridgewater, NJ (US)

(73) Assignee: **Lucent Technologies Inc.**, Murray Hill, NJ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/292,397**

(22) Filed: **Apr. 15, 1999**

(51) **Int. Cl.**[7] **G06F 13/362**
(52) **U.S. Cl.** **710/117**; 710/116; 710/118
(58) **Field of Search** 710/107–118

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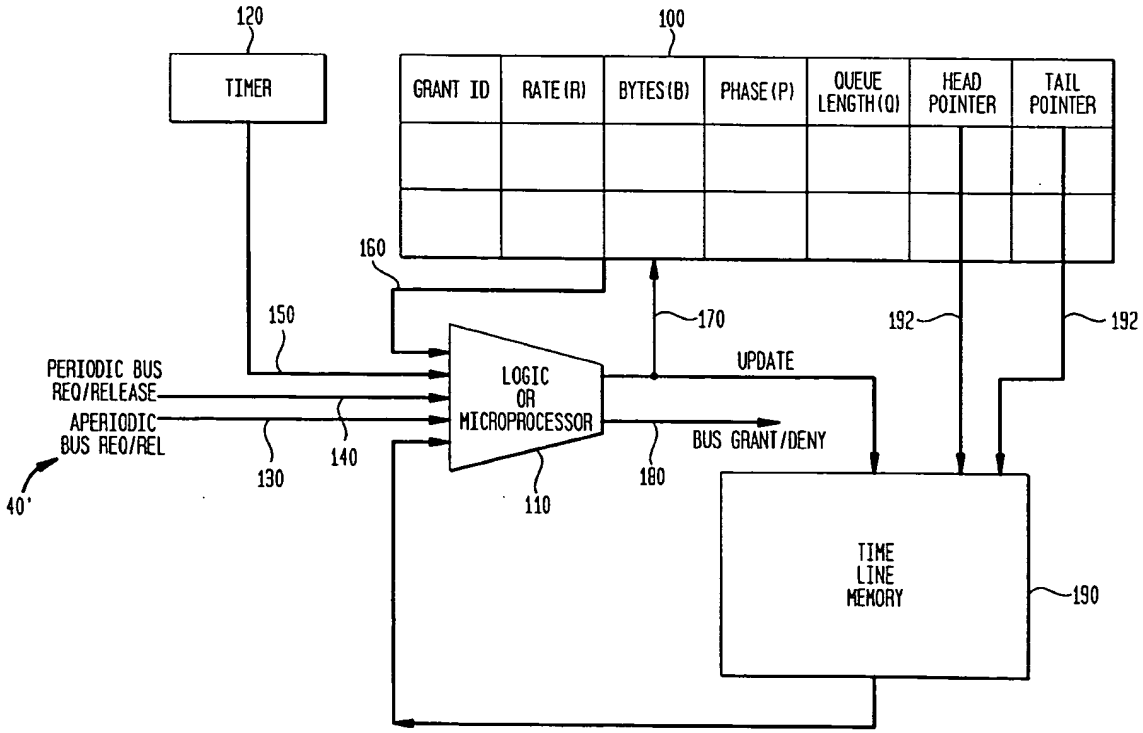
Primary Examiner—Sumati Lefkowitz
(74) *Attorney, Agent, or Firm*—Dickstein Shaprio Morin & Oshinsky LLP

(57) **ABSTRACT**

The invention concerns an arbitration scheme for permitting access to the bus of a computer. The arbitration scheme has the ability to control and reduce the delay experienced by any device by monitoring the queue length of the device and using information concerning the device, such as device rate, phase, data transfer size and queue length. Specifically, the arbiter prevents periodic accessing devices, such as audio and video samplers, from being delayed or interrupted for long periods of time once they have begun accessing the bus.

65 Claims, 6 Drawing Sheets



list tail pointer, however, is now set to the new bottom of the free list, i.e., row **190-*a***. It should be appreciated that any conventional link list method, including reverse and double linked list techniques, could be used to maintain the time line memory **190**.

Bus grants are performed by looking at all of the devices in the service log, accessing the respective time line link list and finding the next grant (i.e., earliest grant in time in the time line memory **190** or alternatively, grants for a device that has a maximum queue length). When the time comes for that service entry, the bus is granted to the device. Once the bus access is complete, the allocated bus access entry is removed from the time line memory (and the device's link list) and also from the service log if all allocations for the same device have been removed. There are various variants of grants. For example, each time a device is granted the bus, the arbiter issue a grant signal. Alternatively, the arbiter can issue a "multi-grant" by issuing a grant signal indicating that the bus has been granted for the next x requests (thus alleviating the need for the device to make requests, since it has already been given x number of grants).

Preferably, the arbiter distinguishes between periodic request that have periods that are sub-multiples of a basic rate (as described above) and periodic requests with periods that are not sub-multiples of the basic rate. When processing periodic requests having periods that are sub-multiples of the basic rate, the arbiter does not have to chain down the time line memory to determine future bus allocations since it is known that the request can be given indefinite service without a conflict. However, when servicing periodic requests having periods that are not sub-multiples of the basic rate, the arbiter must use the time line memory to avoid conflicts since the "non-basic-rate" period cannot be given indefinite service. The basic rate is system dependent and may change accordingly.

Since most peripherals on the market today are not equipped to provide periodic request signals or accept periodic grant signals, the inventor has developed alternate embodiments for implementing the present invention.

One alternative shown in FIG. **6** would be to use an adapter **200**, connected between the peripheral devices **50**, **60** (i.e., device which do not include periodic request or grant lines) and the bus **10**, Which recognizes periodic requests from the devices **50**, **60** and provides appropriate periodic request signals to the arbiter **40'** (via the bus **10**). The adapter **200** would accept signals from, for example the device **50**, on the aperiodic request line which is already part of the device. The adapter **200** would determine based on the attributes of the signal whether the device **50** was requesting periodic or aperiodic access. If the device is granted control of the bus by the arbiter **40'**, the adapter **200** would then provide a grant signal from the arbiter **40'** to the device **50** on the device aperiodic grant line. Since the arbiter **40'** controls processing of all requests whether they be aperiodic or periodic, the grant signal merely needs to identify that the bus is ready to receive information. Put differently, there is only one grant signal for both aperiodic or periodic requests. The inner workings of the arbiter **40'** are the same as described above with reference to the preferred embodiment of the present invention.

Another alternative embodiment includes the adapter **200** within a modified arbiter **40"**, as shown in FIG. **7**, so that extra hardware is not required. Additionally, the devices **50**, **60** can be modified so that the periodic request signals can be multiplexed on the normal (i.e., aperiodic) request lines of the device, along with the aperiodic request signals, so that no extra lines are required. Of course this method involves altering the inside of the peripheral by adding a multiplexer.

While the invention has been described in detail in connection with the preferred embodiments known at the time, it should be readily understood that the invention is not limited to such disclosed embodiments. Rather, the invention can be modified to incorporate any number of variations, alterations, substitutions or equivalent arrangements not heretofore described, but which are commensurate with the spirit and scope of the invention. Accordingly, the invention is not to be seen as limited by the foregoing description, but is only limited by the scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A bus arbitration system comprising:

a processor which accepts periodic and aperiodic bus request signals;

a time line memory connected to said processor for storing information representing bus service duration;

at least one peripheral device connected to said processor for sending bus request signals to said processor, said processor dynamically allocating timeslots for a bus service duration on said bus for said peripheral device based on said periodic and aperiodic request signals by issuing a grant signal to said at least one peripheral device; and

a service log memory connected to said processor for storing information related to said periodic and aperiodic bus request signals and said associated grant signals.

2. The bus arbitration system of claim **1**, wherein said service log also stores information concerning performance metric information of said at least one peripheral device and said processor allocates timeslots based on said performance metric information.

3. The bus arbitration system of claim **2**, wherein said performance metric information is queue length.

4. The bus arbitration system of claim **2**, wherein said service log also stores information about the number of bytes of data associated with each request and information about the period of requests for periodic requests.

5. The bus arbitration system of claim **2**, wherein the processor updates the service log once a request has been granted to indicate that the request has been granted.

6. The bus arbitration system of claim **5**, wherein the update of the service log comprises indicating that a timeslot has been allocated for the granted request.

7. The bus arbitration system of claim **1**, wherein the said at least one peripheral device sends a periodic bus request signal to the processor when the peripheral device is a periodic device.

8. The bus arbitration system of claim **1**, wherein the said at least one peripheral device sends a aperiodic bus request signal to the processor when the peripheral device is an aperiodic device.

9. The bus arbitration system of claim **1**, wherein the processor differentiates between periodic and aperiodic request signals, so that when an aperiodic request is made the processor allocates a timeslot to the at least one device, and when a periodic request is made the processor grants a set of timeslots to the at least one device.

10. The bus arbitration system of claim **2**, wherein the processor utilizes the information stored in the service log memory to dynamically allocate at least one timeslot on the bus to the said at least one device.

39/3,K/37 (Item 37 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014517315 **Image available**
WPI Acc No: 2002-338018/200237
Related WPI Acc No: 2003-706901
XRPX Acc No: N02-265648
Access arbitration method for common bus **in computer systems, involves dynamically adjusting desired weighted bandwidths** assigned **for different** devices **based on measure of data transfer between** devices **over common** bus
Patent Assignee: JEDDELOH J (JEDD-I); MICRON TECHNOLOGY INC (MICR-N)
Inventor: JEDDELOH J
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020002646	A1	20020103	US 98173573	A	19981015	200237 B
			US 2001904632	A	20010713	
US 6473817	B2	20021029	US 98173573	A	19981015	200274
			US 2001904632	A	20010713	

Priority Applications (No Type Date): US 98173573 A 19981015; US 2001904632 A 20010713
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020002646	A1		10	G06F-013/36	Cont of application US 98173573
US 6473817	B2			G06F-013/36	Cont of application US 98173573

Access arbitration method for common bus **in computer systems, involves dynamically adjusting desired weighted bandwidths** assigned **for different** devices **based on measure of data transfer between** devices **over common** bus

Abstract (Basic):
... Desired weighted bandwidths **corresponding** to performance abilities and requirements are **assigned** for primary and secondary **devices** . The **assigned** bandwidths are **dynamically** adjusted during data transfer operation based on the measure of data transfer between the **devices** over a common **bus** .
... a) Program storage **device** ;
(...

...b) Common **bus** access control **apparatus**
...

...For arbitrating access to common **bus** in computer systems...
... **Bus** resources are shared between the **devices** thereby enabling the faster **devices** to have more frequent access to **bus** . Hence, average **amount** of data transferred over the **bus** is increased without allowing the faster **devices** to monopolize the **bus** .

...Title Terms: **BUS** ;
International Patent Class (Main): **G06F-013/36**
International Patent Class (Additional): **G06F-013/362**
Manual Codes (EPI/S-X): **T01-F02C2** ...

... **T01-H05B3** ...

... T01-H07A2 ...

... T01-S03

US006473817B2

(12) **United States Patent**
Jeddeloh

(10) **Patent No.: US 6,473,817 B2**
(45) **Date of Patent: Oct. 29, 2002**

(54) **METHOD AND APPARATUS FOR EFFICIENT BUS ARBITRATION**

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(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/904,632**

(22) Filed: **Jul. 13, 2001**

(65) **Prior Publication Data**

US 2002/0002646 A1 Jan. 3, 2002

Related U.S. Application Data

(63) Continuation of application No. 09/173,573, filed on Oct. 15, 1998.

(51) **Int. Cl.**[7] **G06F 13/36**; G06F 13/362

(52) **U.S. Cl.** **710/113**; 710/116; 710/305; 710/240

(58) **Field of Search** 710/40, 41, 305–315, 710/240–244, 107–119

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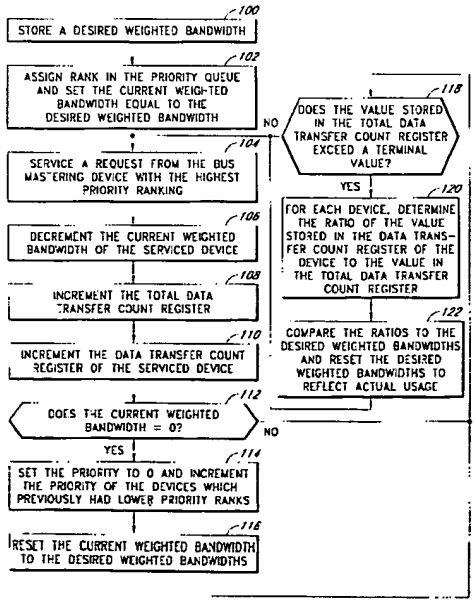
Primary Examiner—Rupal Dharia
(74) *Attorney, Agent, or Firm*—Knobbe Martens Olson & Bear LLP

(57) **ABSTRACT**

A bus arbitration regulates access to a common bus by a plurality of devices by assigning each device a priority rank. A current weighted bandwidth of each device is set equal to a desired weighted bandwidth. A request to access the common bus is granted to the device having the highest priority rank among a set of requesting devices. The current weighted bandwidth the first device is decremented. The priority rank of the serviced device is set equal to a lowest value if its current weighted bandwidth is equal to a minimum value. The priority rank of a set of devices which previously had a lower priority rank than the first device is increased. The current weighted bandwidth of the serviced device is set equal to the desired weighted bandwidth. After a number of bus transactions have been completed, the desired weighted bandwidth of the devices may be adjusted to based upon system performance.

21 Claims, 3 Drawing Sheets



The third time that the bus arbiter polls for requests for bus resources, again the devices 3 and 5 are each requesting service. Because device 3 has the highest priority of the two, it is serviced. State 4 illustrates the state of the system after the device 3 has been serviced. The weighted bandwidth of the device 2 has been decremented from 1 to 0.

In State 4, the weighted bandwidth of the device 3 has reached the minimum value of 0. Therefore, the priority of the device 3, 4, 5 and 6 change. State 5 illustrates the state of the system after these priorities have been changed. The priority of device 3 is set to 0 and the priority of device 4 has been increased from 2 to 3. The priority of device 5 has been increased from 1 to 2 and the priority of device 6 has been increased from 0 to 1. The current weighted bandwidth of the device 3 has been reset to the desired weighted bandwidth value of 2.

The fourth time that the bus arbiter polls for requests for bus resources, the devices 3 and 5 are each requesting service. Because device 5 now has a higher priority than device 3, it is serviced next. State 6 illustrates the state of the system after the device 5 has been serviced. The weighted bandwidth of the device 5 has been decremented from 2 to 1. The priority of all devices remains unchanged.

A myriad of alternative embodiments will be readily apparent to one skilled in the art based upon the disclosure herein. The invention may be applied to a Peripheral Components Interconnect (PCI) bus, other well known buses or later developed bus protocols. The bus may be located within a personal computer, a network computer or any other manner of electronic equipment where multiple units compete for limited communication resources.

The invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiment is to be considered in all respects only as illustrative and not restrictive and the scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

What is claimed is:

1. A method of arbitrating access to a common bus comprising:

assigning a desired weighted bandwidth to a first device which transfers data over the common bus, wherein said desired weighted bandwidth reflects selected performance abilities and requirements of said first device;

assigning a desired weighted bandwidth to a second device which transfers data over the common bus, wherein said desired weighted bandwidth reflects selected performance abilities and requirements of said second device;

arbitrating access to the common bus based upon the desired weighted bandwidths of the first and second devices; and

dynamically adjusting the desired weighted bandwidths of the first and second devices during operation based upon a history of a measure of data transfer over the common bus by at least one of the first and second devices, occurring within a defined period.

2. The method of claim 1 wherein the history of the measure of data transfer over the common bus comprises the number of data transfers made by one of the first and second devices.

3. A program storage device storing instructions that when executed by a computer perform the method comprising:

assigning a desired weighted bandwidth to a first device which transfers data over the common bus, wherein said desired weighted bandwidth reflects selected performance abilities and requirements of said first device;

assigning a desired weighted bandwidth to a second device which transfers data over the common bus, wherein said desired weighted bandwidth reflects selected performance abilities and requirements of said second device;

arbitrating access to the common bus based upon the desired weighted bandwidths of the first and second devices; and

dynamically adjusting the desired weighted bandwidths of the first and second devices during operation based upon a history of a measure of data transfer over the common bus by at least one of the first and second devices, occurring within a defined period.

4. The program storage device of claim 3 wherein the history of the measure of data transfer over the common bus comprises the number of data transfers made by one of the first and second devices.

5. A program storage device storing instructions that when executed by a computer perform the method comprising:

assigning each of a plurality of devices a priority rank;

setting a current weighted bandwidth of each of said plurality of devices equal to a desired weighted bandwidth;

servicing a request to access a common bus from a first device of said plurality of devices, said first device having the highest priority rank among a set of requesting devices;

decrementing said current weighted bandwidth of said first device;

setting said priority rank of said first device equal to a lowest value if said decremented current weighted bandwidth of said first device is equal to a minimum value and increasing said priority rank of a set of devices which previously had a lower priority rank than said first device;

setting said current bandwidth of said first device equal to said desired weighted bandwidth; and

dynamically adjusting said desired weighted bandwidth of said first device during operation based upon a history of actual usage of said common bus by said first device, wherein said history comprises a record of bus accesses granted to said first device, and a record of bus accesses granted to others of said plurality of devices, occurring within a defined period.

6. The program storage device of claim 5 wherein said desired weighted bandwidth is different for different devices of said plurality of devices.

7. The program storage device of claim 5 wherein said desired weighted bandwidth of said first device is representative of a rate at which said first device transfers data over said common bus.

8. The program storage device of claim 5 wherein said desired weighted bandwidth of each of said plurality of devices is updated based upon actual usage of said common bus.

9. The program storage device of claim 5 wherein the instructions for dynamically adjusting said desired weighted bandwidth further comprises instructions that when executed by a computer perform the method comprising:

determining a total number of serviced requests corresponding to all of said plurality of devices;

determining a total number of serviced requests corresponding to said first device; and

determining a new desired weighted bandwidth for said first device based upon a ratio of said total number of serviced requests corresponding to said first device with respect to said total number of serviced requests corresponding to all of said plurality of devices.

39/3,K/63 **(Item 63 from** file: 350)
DIALOG(R)File 350:Derwent WPIX

012409069 **Image available**
WPI Acc No: 1999-215177/199918
XRPX Acc No: N99-158342
Interconnection circuit **for** electronic **modules**
Patent Assignee: FLEXTEL SPA (FLEX-N); UNITEL SRL (UNIT-N)
Inventor: DONDOLINI A
Number of Countries: 083 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9913407	A1	19990318	WO 98IT238	A	19980828	199918	B
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			WO 98IT238	A	19980828		
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AU 753341	B	20021017	AU 9891838	A	19980828	200280	

Priority Applications (No Type Date): IT 97TO796 A 19970908
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9913407	A1	E	14	G06F-013/40	

Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9891838	A			Based on patent WO 9913407
EP 1015990	A1	E	G06F-013/40	Based on patent WO 9913407

Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI NL PT SE

IT 1294849	B		H05K-000/00	
EP 1015990	B1	E	G06F-013/40	Based on patent WO 9913407

Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI NL PT SE

DE 69802206	E		G06F-013/40	Based on patent EP 1015990
				Based on patent WO 9913407
ES 2166616	T3		G06F-013/40	Based on patent EP 1015990
AU 753341	B		G06F-013/40	Previous Publ. patent AU 9891838
				Based on patent WO 9913407

Interconnection circuit **for** electronic **modules**

Abstract (Basic):
... A support has a **number** of **electrical connection** points which forms a data and/or command **bus** and is **connected** to **connectors** each of which is suitable for accommodating an electronic module e.g. system or **peripheral** modules.
... A **circuit** (10) **interconnects electronic** modules in a data

and/or command channels channel (**bus**) **segment** , and includes **connectors** (11-1-11-5) which accommodate electronic modules of the same type of different types, and a **number** of **pins** (14) associated with the **connectors** and interconnected through a **number** of **electrical connections** (21). The **connections** (21) between the **pins** (14) of the **connectors** (11-1-11-5) are controlled by electronic switches (24-1-24-4) in such a way that a **number** of sub- **segments** , each comprising a subset of **connectors** (11-1-11-5), is obtained from a **bus segment** . The **connections** (21) are formed such that different types of electronic modules can be accommodated e.g. system modules and **peripheral** modules, in any position of the **bus segment** . An INDEPENDENT CLAIM is included for an **interconnection circuit** for system and **peripheral** modules...

... **Interconnection circuit** in compliance with **PCI data** and commands **channel** specifications...

...Provides **bus segment dynamically** configurable into numerous **bus segments** or sub- **segments** , each comprising a subset of **total number** of slots included in the **bus segment** .

...

...The drawing shows a logic diagram of the **connections** for clock signals **according** to the invention...

... **Connectors** (11...

... **Pins** (14...

... **Electrical connections** (21...

... **Interface** (27

Technology Focus:

... The **interconnection circuit** is made in compliance with **PCI data** and commands **channel** specifications (CompactPCI (RTM)) as defined by the PICMG (**PCI** Industrial Computers Manufacturers Group).

International Patent Class (Main): **G06F-013/40** ...

Manual Codes (EPI/S-X): **T01-C07** ...

... **T01-H07A1**

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(43) International Publication Date: 18 March 1999 (18.03.99)

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(22) International Filing Date: 28 August 1998 (28.08.98)

(30) Priority Data:
TO97A000796 8 September 1997 (08.09.97) IT

(71) Applicant *(for all designated States except US)*: FLEXTEL S.P.A. [IT/IT]; Corso Vercelli, 328, I–10015 Ivrea (IT).

(72) Inventor; and

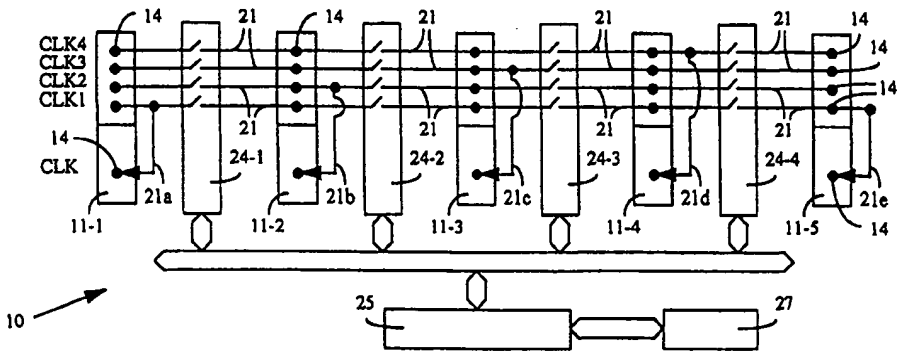
(75) Inventor/Applicant *(for US only)*: DONDOLINI, Alessandro [IT/IT]; Via Bozzo Costa, 107/7, I–16035 Rapallo (IT).

(74) Agent: CASUCCIO, Carlo; Olivetti S.p.A., Via Jervis, 77, I–10015 Ivrea (IT).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: INTERCONNECTION CIRCUIT FOR ELECTRONIC MODULES



(57) Abstract

This invention relates to a circuit (10) for interconnecting electronic modules in a data and/or commands channel (bus) segment. The circuit (10) comprises a plurality of connectors (11–1÷11–5) designed to accommodate electronic modules of the same type or different types and a plurality of Pins (14) associated with the connectors and interconnected through a plurality of electric connections (21). The electric connections (21) between the Pins (14) of the connectors (11–1÷11–5) are controlled by electronic switches (24–1÷24–4) in such a way that a plurality of sub–segments, each comprising a subset of the connectors (11–1÷11–5), is obtained from a bus segment. Moreover the connections (21) are made in such a way that it is possible to accommodate the different types of electronic modules, for example system modules and peripheral modules, in any position of the bus segment.

CLAIMS

1. Interconnection circuit for electronic modules comprising

- a support (12) having a plurality of electric connection points (14) and suitable for constituting a data and/or commands channel (bus) segment,

- a plurality of connectors (11-1÷11-5) connected to said connection points (14) and each suitable for accommodating a corresponding electronic module, and

- interconnection means (21÷23) for connecting said connection points (14) to each other; characterized in that

- electronic switching means (24-1÷24-4) are provided for selectively interrupting the connection made by said interconnection means (21÷23) and selectively obtaining from said bus segment a plurality of sub-segments, each comprising a subset of said connectors (11-1÷11-5).

2. Interconnection circuit according to claim 1 characterized in that

- control means (25) are provided for selectively controlling said electronic switching means (24-1÷24-4).

3. Interconnection circuit for electronic modules, both system and peripheral type, suitable for exchanging point-to-point type signals (CLK#, INT#, REQ#, GNT#), comprising

- a support (12) having a plurality of electric connection points (14),

- a plurality of connectors (11-1÷11-5) connected to said connection points (14) and suitable for accommodating at least one electronic system module and a plurality of electronic peripheral modules, and

- interconnection means (21÷23) connecting given connection points together in order to permit the exchange of said point-to-point type signals (CLK#, INT#, REQ#, GNT#); characterized in that

- said interconnection means (21÷23) are arranged in such a way that said system module is connected to all the peripheral modules in order to permit the exchange of said point-to-point type signals (CLK#, INT#, REQ#, GNT#) between said system module and each of said peripheral modules, regardless of the position of the connector (11-1÷11-5) wherein said system module is accommodated.

4. Interconnection circuit according to claim 3 characterized in that

- said point-to-point type signals (CLK#, INT#, REQ#, GNT#) comprise timing or clock signals, interrupt signals, exchange request signals and signals acknowledging said exchange request signals.

5. Interconnection circuit according to claim 3 wherein said support (12) with said plurality of connection points (14) is suitable for constituting a data and/or commands channel (bus) segment, characterized in that

- electronic switching means (24-1÷24-4) are provided for selectively interrupting the connection made by said interconnection means (21÷23) and selectively obtaining from said bus segment a plurality of sub-segments, each comprising a subset of said connectors (11-1÷11-5).

6. Interconnection circuit according to claim 5 characterized in that

- control means (25) are provided for selectively controlling said electronic switching means (24-1÷24-4).

39/3,K/70 (Item 70 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011813173 **Image available**
WPI Acc No: 1998-230083/199820
XRPX Acc No: N98-182233
Switching hub using asynchronous transfer mode switch as back-plane bus - dynamically **controls** bus **arbitration i.e.** allocation **of bandwidth, on** bus **for autonomous ATM and LAN switching modules** coupled **to it is dynamically controlled** according **to various modules**
Patent Assignee: BAY NETWORKS INC (BAYN-N)
Inventor: NOLL M; PRINCE J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5734656	A	19980331	US 95501476	A	19950712	199820 B
			US 95537144	A	19950929	

Priority Applications (No Type Date): US 95501476 A 19950712; US 95537144 A 19950929
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5734656	A		16	H04L-012/28	Cont of application US 95501476

Switching hub using asynchronous transfer mode switch as back-plane bus - ...

... dynamically **controls** bus **arbitration i.e.** allocation **of bandwidth, on** bus **for autonomous ATM and LAN switching modules** coupled **to it is dynamically controlled** according **to various modules**

...Abstract (Basic): The **apparatus** for **dynamically allocating** bandwidth on a time division multiplexed (TDM) **bus** among a **number** of modules **coupled** to it, has a memory array having a **number** of entries. Each entry stores a module identification **number** identifying one of the modules. A controller is **coupled** to the memory array, and writes the module identification **number** to at least one of the entries in the memory array in accordance with an algorithm executed by the controller to dynamically select the module identification **number** written to each of the entries...

...The controller sequentially reads the entries in the memory array, and reads the module identification **number** from one of the entries each time division and **allocates** bandwidth on the TDM **bus** to the module identified by the module identification **number** read from one of the entries...
...ADVANTAGE - Improves efficiency and predictability of **allocation** . Uses bandwidth across ATM core fabric of ATM switch. Allows time division multiplexing of **bus** under program control such that each module, e.g. Ethernet or Token Ring module, is allowed desired **number** of cell slots on **bus** during which to transfer data...
...Title Terms: **BUS** ;

US005734656A

United States Patent [19]

Prince et al.

[11] Patent Number: 5,734,656

[45] Date of Patent: Mar. 31, 1998

[54] **METHOD AND APPARATUS FOR DYNAMICALLY ALLOCATING BANDWIDTH ON A TDM BUS**

[75] Inventors: **Jeff Prince**, Sunnyvale; **Mike Noll**, San Jose, both of Calif.

[73] Assignee: **Bay Networks, Inc.**, Santa Clara, Calif.

[21] Appl. No.: **537,144**

[22] Filed: **Sep. 29, 1995**

Related U.S. Application Data

[63] Continuation of Ser. No. 501,476, Jul. 12, 1995, abandoned.

[51] **Int. Cl.**[6] **H04L 12/28**

[52] **U.S. Cl.** **370/401**; 370/395; 370/362

[58] **Field of Search** 370/362, 398, 370/399, 400, 401, 402, 404, 423, 434, 439, 458, 468, 452, 455, 466, 395, 397

[56] **References Cited**

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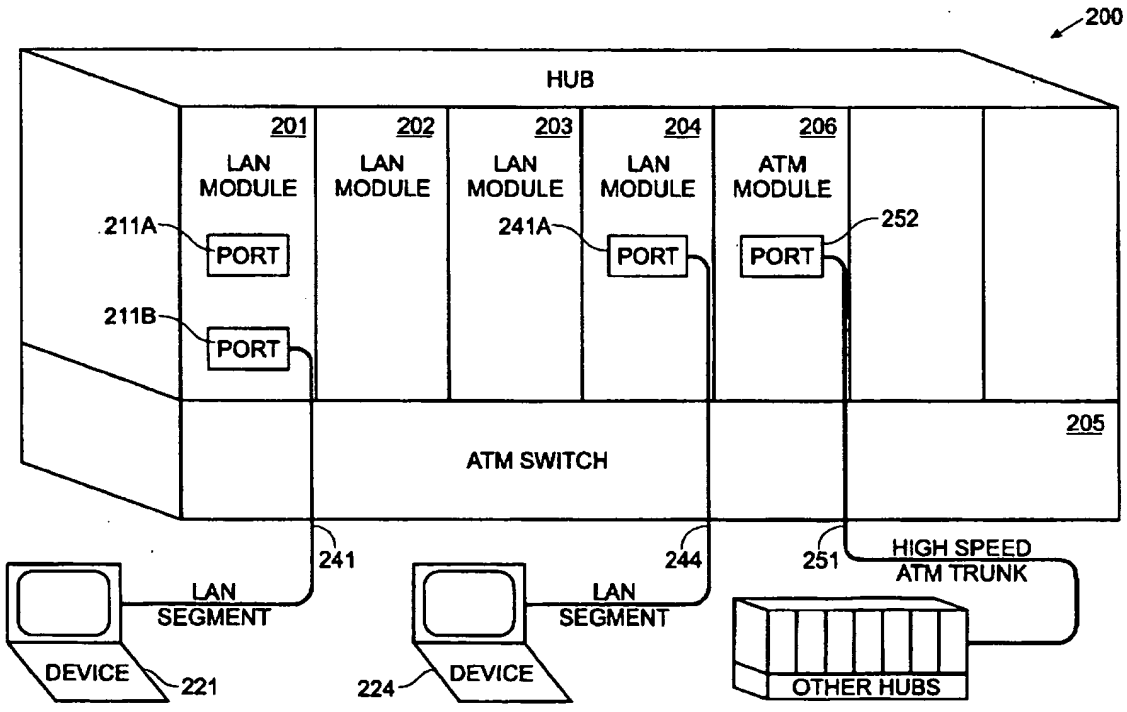
5,491,694	2/1996	Oliver et al.	370/455

Primary Examiner—Wellington Chin
Assistant Examiner—Soon-Dong Hyun
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman, LLP

[57] **ABSTRACT**

The present invention relates to methods and apparatus providing for a switching hub in which an asynchronous transfer mode (ATM) switch is utilized as a backplane bus. Bus arbitration, i.e., allocation of bandwidth, on the bus for autonomous ATM and LAN switching modules coupled thereto is dynamically controlled according to the needs of the various modules. In particular, the present invention allows time division multiplexing of the bus under programmatic control such that each module, e.g., an Ethernet or Token Ring module, is allowed a desired number of cell slots on the bus during which to transfer data, which the module has translated into ATM cells, across the bus.

5 Claims, 6 Drawing Sheets



(RID) **605** and a DTAG **606**, prior to transmission across the backplane bus **370**. The DTAG specifies the destination LAN module and port number to which the cell is to be transmitted, while the RID is used by the SAR module in the receiving LAN module to reassemble cells having the same RID in order to transfer the entire packet to the appropriate port therein. Such a RID is useful when a receiving LAN module receives cells concurrently from multiple circuits. Without the RID to identify which cells should be reassembled into a packet, data corruption is likely to occur.

The concept of a routing tag (DTAG) **606** is well known to those of ordinary skill in the art. However, such routing information is generally a single value whose range depends simply on the length of the routing tag field. The present invention subdivides the DTAG **606** into two components as illustrated in FIG. **9**, wherein the lower 8 bits of the DTAG comprise a destination port number **903** (low order nibble—bits 0–3) and a destination module number **902** (high order nibble), and the uppermost nibble specifies a multicast group number **901**, such that any DTAG value between 0 to 255 (FF hex) is a unicast number **904** that uniquely identifies a particular port on a particular LAN module, allowing unicast cells to be switched in a connectionless fashion, and any DTAG value between 256 (100 hex) to 4095 (111 hex) is a multicast group number that identifies a group of ports on any number of LAN modules. A multicast group number mask in each LAN module is configured to recognize a particular multicast group number, and thus, receive cells in which the multicast group number is used.

Conclusion

There are, of course, alternatives to the described embodiment which are within the understanding of one of ordinary skill in the relevant art. The present invention is intended to be limited only by the claims presented below.

Thus, what has been described is a method and apparatus which utilizes an ATM switch backplane bus for interconnecting LAN and ATM modules in which the ATM switch allocates bandwidth to the switching modules using a dynamically computed algorithm that is based on application priorities, total bandwidth requirements, and fairness, and in which a pipelining mechanism enhances utilization of the autonomous switching modules as well as bandwidth on the backplane, and in which routing of ATM cells between modules is accomplished under certain conditions without establishing a permanent virtual circuit between the modules.

What is claimed is:

1. An apparatus for dynamically allocating bandwidth on a time division multiplexed (TDM) bus among a plurality of modules coupled thereto, comprising:

a memory array having a plurality of entries, each entry for storing therein a module identification number identifying one of said plurality of modules;

a controller coupled to said memory array, said controller writing said module identification number identifying one of said plurality of modules to at least one of said plurality of entries in said memory array in accordance with an algorithm executed by said controller to dynamically select said module identification number written to each of said plurality of entries, and

said controller sequentially reading said plurality of entries in said memory array, said controller reading said module identification number from one of said plurality of entries each time division and allocating bandwidth on said TDM bus to said module identified by said module identification number read from said one of said plurality of entries.

2. An apparatus for dynamically allocating bandwidth on a time division multiplexed (TDM) bus to a module coupled thereto, comprising:

a memory array having a plurality of entries, each for storing therein a module identification number identifying one a plurality of modules;

a controller coupled to said memory array, said controller writing said module identification number identifying one of said plurality of modules to at least one of said plurality of entries in said memory array in response to an algorithm executed by said controller for dynamically selecting said module identification number written to each of said plurality of entries; and

said controller sequentially reading said module identification number from one of said plurality of entries each time division and allocating one time division on said TDM bus to said module if said module identification number read from said one of said plurality of entries identifies said module.

3. An apparatus for dynamically allocating a slot of time on a time division multiplexed (TDM) bus to a module coupled thereto, comprising:

an ownership bus coupled to said module for transmitting a module identification number identifying one of a plurality of modules to said module;

a memory array coupled to said ownership bus, said memory array having multiple entries, each said entry capable of storing therein said module identification number identifying one of said plurality of modules; and

a controller coupled to said memory array, said controller executing a program for dynamically updating at least one of said multiple entries with said module identification number identifying said module,

said controller reading a module identification number from one of said multiple entries each said slot of time and transmitting said module identification number over said ownership bus, thereby notifying said module that it has been allocated said slot of time on said TDM bus if said module identification number transferred on said ownership bus identifies said module.

4. A method of dynamically allocating bandwidth on a time division multiplexed (TDM) bus among a plurality of modules coupled thereto, comprising the steps of:

dynamically writing one of a plurality of values to at least one of a plurality of entries in a memory array, said plurality of values each indicating a module identification number identifying one of said plurality of modules;

sequentially reading through said plurality of entries in said memory array, one entry each time division;

driving said value onto an ownership bus coupled to said plurality of modules;

comparing at each said module said value on said ownership bus to said module identification number identifying said module; and

allocating said bandwidth on said TDM bus to said module if said value on said ownership bus is identical to said module identification number identifying said module.

39/3,K/54 (Item 54 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013052622 **Image available**
WPI Acc No: 2000-224477/200019
XRPX Acc No: N00-168205
Resource allocating method involves allocating **fixed or** dynamic **resource for** data **transmission** connection **based on quality of service class**
Patent Assignee: NOKIA MOBILE PHONES LTD (OYNO)
Inventor: KALLIOKULJU J; TURUNEN M
Number of Countries: 087 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200010334	A2	20000224	WO 99FI643	A	19990729	200019 B
AU 9951661	A	20000306	AU 9951661	A	19990729	200030
FI 9801728	A	20000327	FI 981728	A	19980810	200031
FI 105641	B1	20000915	FI 981728	A	19980810	200054
EP 1104610	A2	20010606	EP 99936635	A	19990729	200133
			WO 99FI643	A	19990729	
US 6553006	B1	20030422	US 99370737	A	19990809	200330

Priority Applications (No Type Date): FI 981728 A 19980810
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200010334	A2	E	26	H04Q-000/00	
Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZA ZW					
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW					
AU 9951661	A			H04Q-000/00	Based on patent WO 200010334
FI 9801728	A			H04Q-011/04	
FI 105641	B1			H04Q-011/04	Previous Publ. patent FI 9801728
EP 1104610	A2	E		H04L-012/56	Based on patent WO 200010334
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
US 6553006	B1			H04B-007/00	

Resource allocating method involves allocating **fixed or** dynamic **resource for** data **transmission** connection **based on quality of service class**

Abstract (Basic):
... The fixed resource or **dynamic** resource is **allocated** for **data** transmission **connection** based on quality of service class in which information to be transmitted in **data** transmission **connection** is classified.
... The information to be transmitted is processed **according** to protocol stack which contains LLC layer and RLC/MAC layer. The RLC block (209...

...item of information classified into such quality of service class for which fixed resource is **allocated** . The common RLC block (211) is provided for processing information classified into all the other...

...packets. The data packets coming from upper layers of protocol stack to LLC layer are **divided** into different LLE blocks based on quality of service requirement defined for each quality. An INDEPENDENT CLAIM is also included for resources **allocating device** .

...

...For **allocating** resources for establishing data communication between **wireless** communication **device** and mobile communication network especially for global system for mobile communication system, GSM mobile communication...

...The resource **allocation** is **divided** into fixed and **dynamic allocation** on based judgment result indicating **real time** packet **connection** or non-real time packet **connection** . Thereby secures reliable fast packet transmission when compared with **dynamic** resource **allocation** .

...Title Terms: **ALLOCATE** ;

US006553006B1

(12) **United States Patent**
Kalliokulju et al.

(10) **Patent No.: US 6,553,006 B1**
(45) **Date of Patent: Apr. 22, 2003**

(54) **RESOURCE ALLOCATION IN PACKET-FORMAT DATA TRANSMISSION**

(75) Inventors: **Juha Kalliokulju**, Vesilahti (FI); **Matti Turunen**, Tampere (FI)

(73) Assignee: **Nokia Mobile Phones Limited**, Espoo (FI)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/370,737**

(22) Filed: **Aug. 9, 1999**

(30) **Foreign Application Priority Data**

Aug. 10, 1998 (FI) 981728

(51) **Int. Cl.**[7] **H04B 7/00**
(52) **U.S. Cl.** **370/310**; 370/337
(58) **Field of Search** 370/310, 314, 370/321, 329, 337, 341, 347, 437, 442, 465, 468; 455/450, 451, 452

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Finnish Office Action.

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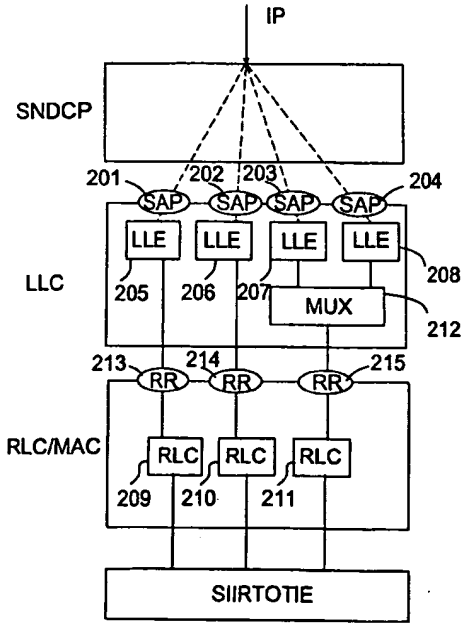
Primary Examiner—Dang Ton
Assistant Examiner—Frank Duong
(74) *Attorney, Agent, or Firm*—Perman & Green, LLP

(57) **ABSTRACT**

The invention relates to a method for allocating resources for a data transmission connection between a wireless communication device and a mobile communication network. In the method, the information to be transmitted is divided into at least a first and a second quality of service class. For the data transmission connection, either a fixed resource or a dynamic resource is allocated on the basis of the quality of service class in which the information to be transmitted in the data transmission connection is classified.

14 Claims, 3 Drawing Sheets



single-stage activation, wherein merely a channel request message is transmitted from the wireless communication device MS, wherein the carrier service block in the base station system determines, on the basis of the service access point identifier transmitted in this message, the type of the resource requested for the packet connection. Correspondingly, resources for the fourth packet connection are activated with either two-stage or single-stage signalling. In these third and fourth packet connection set-ups, the resource allocation request is processed in the third RLC block **211**.

In the hardware used in current mobile communication systems, it is possible to implement the RLC and LLE blocks according to the invention and their functionality with modifications in the software, primarily in sections of the implementation of protocol stacks.

The present invention is not restricted solely to the above-presented embodiments, but it can be modified within the scope of the appended claims. The invention can also be applied for example in the UMTS system (Universal Mobile Telecommunication System).

What is claimed is:

1. A method for allocating resources for a data transmission connection between a wireless communication device and a mobile communication network comprising:

dividing information to be transmitted on the basis of a quality of service class to be used for transmission;

allocating a fixed resource for the data transmission connection for information having a quality of service class for which a fixed resource is to be utilized; and

allocating a dynamic resource for the data transmission connection for information having a quality of service class for which a dynamic resource is to be utilized.

2. The method according to claim **1**, further comprising:

processing information having the quality of service class for which a fixed resource is utilized in one RLC block of an RLC/MAC layer; and

processing information having all other quality of service classes in a common RLC block of an RLC/MAC layer.

3. The method according to claim **2**, wherein the information is transmitted in packets, the method further comprising dividing data packets coming from upper layers of a protocol stack to an LLC layer into different LLE blocks on the basis of quality of service requirements defined for each packet.

4. The method according to claim **1**, further comprising utilizing the wireless communication device to identify the quality of service class in the mobile communication network.

5. The method according to claim **4**, further comprising:

attaching an LLC service access point identifier to each quality of service class, and;

identifying the quality of service class in the mobile network by transmitting the LLC service access point identifier assigned to the quality of service class.

6. The method according to claim **1**, further comprising allocating a fixed resource for the data transmission connections in which data transmission is performed substantially in real time.

7. A communication device for processing and transmitting information to be transmitted in packet form in one or more data transmission connections, the communication device comprising:

circuitry for dividing the information on the basis of a quality of service class to be used for transmission; and

means for allocating resources for each said data transmission connection on the basis of the quality of service class in which the information to be transmitted in the data transmission connection is divided, wherein the means for allocating resources comprise means for fixed resource allocation and means for dynamic resource allocation.

8. The communication device according to claim **7**, characterized in that it comprises means for processing information according to a protocol stack, which contains at least an LLC layer and an RLC/MAC layer, and that the means (**209, 210**) for fixed resource allocation and the means (**211**) for dynamic resource allocation are established in the RLC/MAC layer.

9. The communication device according to claim **8**, characterized in that it comprises means for identifying a quality of service class in the mobile communication network.

10. A communication system, in which information is arranged to be transmitted in packet form in one or more data transmission connections between a wireless communication device (MS) and a mobile communication network, the communication system comprising:

circuitry for dividing the information on the basis of a quality of service class to be used for transmission;

means for allocating resources for each said data transmission connection on the basis of the quality of service class in which the information to be transmitted in the data transmission connection is divided, wherein the means for allocating resources comprise means for fixed resource allocation and means for dynamic resource allocation.

11. A method for allocating resources for a data transmission connection between a wireless communication device and a mobile communication network comprising:

dividing information to be transmitted on the basis of a quality of service class to be used for transmission;

allocating a fixed resource for the data transmission connection for information having a first quality of service class; and

allocating a dynamic resource for the data transmission connection for information having another quality of service class.

12. The method according to claim **1**, further comprising:

processing information having the first quality of service class in one RLC block of an RLC/MAC layer; and

processing information having all other quality of service classes in a common RLC block of an RLC/MAC layer.

13. The method according to claim **12**, wherein the one RLC block requests allocation of the fixed resource from the mobile communication network.

14. The method according to claim **12**, wherein the common RLC block requests allocation of the dynamic resource from the mobile communication network.

* * * * *

39/3,K/47 (Item 47 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013913098 **Image available**
WPI Acc No: 2001-397311/200142
Related WPI Acc No: 2000-283371; 2001-367189
XRPX Acc No: N01-292788

Dynamic **bandwidth negotiation scheme for** wireless **computer networks, involves** allocating **bandwidth in spread spectrum communication channel of computer network, based on bandwidth requests of** devices **within network**

Patent Assignee: SHAREWAVE INC (SHAR-N); EKAMBARAM N (EKAM-I); GUBBI R R (GUBB-I); NGUYEN B (NGUY-I)
Inventor: EKAMBARAM N; GUBBI R R; NGUYEN B
Number of Countries: 094 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200106710	A1	20010125	WO 2000US19985	A	20000720	200142 B
AU 200063649	A	20010205	AU 200063649	A	20000720	200142
EP 1195026	A1	20020410	EP 2000950559	A	20000720	200232
			WO 2000US19985	A	20000720	
US 20020133589	A1	20020919	US 98151579	A	19980911	200264
			US 99357462	A	19990720	
KR 2002029427	A	20020418	KR 2002700802	A	20020119	200269
CN 1361962	A	20020731	CN 2000810607	A	20000720	200279
JP 2003505930	W	20030212	WO 2000US19985	A	20000720	200321
			JP 2001511037	A	20000720	
MX 2002000665	A1	20041001	WO 2000US19985	A	20000720	200557
			MX 2002665	A	20020118	

Priority Applications (No Type Date): US 99357462 A 19990720; US 98151579 A 19980911
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200106710	A1	E	19	H04L-012/28	
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW					
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TZ UG ZW					
AU 200063649	A			H04L-012/28	Based on patent WO 200106710
EP 1195026	A1	E		H04L-012/28	Based on patent WO 200106710
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
US 20020133589	A1			G06F-015/173	CIP of application US 98151579
KR 2002029427	A			H04L-012/28	
CN 1361962	A			H04L-012/28	
JP 2003505930	W		26	H04L-012/28	Based on patent WO 200106710
MX 2002000665	A1			H04L-012/28	Based on patent WO 200106710

Dynamic **bandwidth negotiation scheme for** wireless **computer networks, involves** allocating **bandwidth in spread spectrum communication channel of computer network, based on bandwidth requests of** devices **within network**

Abstract (Basic):

... The **dynamic** bandwidth negotiation scheme involves **dynamically allocating** bandwidth within a spread spectrum communication channel of computer network, based on bandwidth requests of **devices** within the computer network.

... The method involves **dynamically allocating** bandwidth **according** to priority of requests of **devices** within the computer network. The priorities of the requests are arranged such that bandwidth requests associated with isochronous transmission within the network are accorded highest priority. A table of bandwidth **allocations** is maintained by server of computer network, so as to account for a bandwidth utilization within the network. The table is **dynamically** updated **according** to bandwidth requests by the **devices** and **allocations** made in accordance with the requests...

...For **dynamically allocating** bandwidth use between server and other associated network clients within spread spectrum communication channel of **wireless** computer network and other network environments...

...Reduces difficulties and cost associated with **wire** communication **links** , by incorporating the table of bandwidth **allocations** , which is **dynamically** updated **according** to bandwidth requests...

...Title Terms: **WIRELESS** ;

International Patent Class (Main): **G06F-015/173** ...

Manual Codes (EPI/S-X): **T01-C03C** ...

... **T01-H07C5A** ...

... **T01-M02A1B**

US 20020133589A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2002/0133589 A1

GUBBI et al. (43) Pub. Date: Sep. 19, 2002

(54) DYNAMIC BANDWIDTH NEGOTIATION SCHEME FOR WIRELESS COMPUTER NETWORKS

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LOS ANGELES, CA 90025 (US)

(*) Notice: This is a publication of a continued prosecution application (CPA) filed under 37 CFR 1.53(d).

(21) Appl. No.: 09/357,462

(22) Filed: Jul. 20, 1999

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/151,579, filed on Sep. 11, 1998.

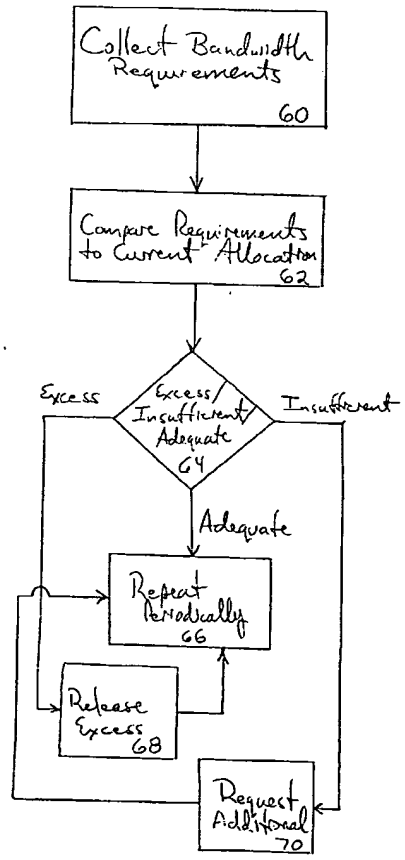
Publication Classification

(51) Int. Cl.[7] G06F 15/173

(52) U.S. Cl. 709/225

(57) ABSTRACT

Bandwidth within a communication channel of a computer network is dynamically allocated according to bandwidth requests of devices within the computer network. Such requests may include releases of excess bandwidth in addition to requests for additional bandwidth. In some cases, the communication channel may be a wireless, spread spectrum communication channel. In general, the bandwidth may be dynamically allocated according to priorities of the requests. For example, the requests may be arranged such that those associated with isochronous transmissions within the computer network are accorded the highest priority. A table of such bandwidth allocations may be maintained (e.g., by a network master device) so as to account for bandwidth utilization within the network. Such a table may include bandwidth allocations for the various information streams according to their varying priorities. The table may then be dynamically updated according to the bandwidth requests and any bandwidth allocations made in accordance therewith.



available bandwidth for the subnet. If the currently allocated bandwidth already equals the available bandwidth (after taking into account any bandwidth being released by any of the network clients) requests for additional are rejected and the respective client devices are so notified. If, however, additional bandwidth is available, requests for additional bandwidth are allocated as follows. First, requests for additional bandwidth to transport isochronous streams are allocated. If additional bandwidth is still available after these requests have been satisfied, the requests for high, medium and low priority streams are visited in that order. Within any of the stream priority levels, the bandwidth is allocated in the following order of priority:

[0032] 1. Requests from the device with the current overall lowest bandwidth allocation are satisfied first;

[0033] 2. Requests from the device with lowest current bandwidth allocation for the current priority level are satisfied next; and

[0034] 3. The remaining requests are satisfied on a first-come-first-serve basis.

[0035] For purposes of the present bandwidth allocation scheme, the master device maintains a table listing the allocated bandwidth (e.g., in Mbits/sec) for each stream priority level at every client device, the requested bandwidth for each stream priority at every device and the time of the request as shown in Table 1. These values can be compared against the actual available bandwidth (which may be stored separately or in the same table in a separate entry) when new requests for bandwidth are made and/or when excess bandwidth is released. Each time new requests are made/satisfied and/or when excess bandwidth is released, the bandwidth allocation table (which may be stored in memory at the host **13** or server **12**) is updated. For bandwidth allocation purposes, the requirements of master device are treated that same as those for any other device in a subnet.

TABLE 1

Device	Priority Level	Allocated Bandwidth (Mbps)	Required Bandwidth (Mbps)	Time of Request
Device 0 (Master)	Isochronous High Medium Low			
Device 1 (Client 1)	Isochronous High Medium Low			
			•	
			•	
			•	
Device N (Client N)	Isochronous High Medium Low			

[0036] To summarize the above processes, each network device periodically assesses its bandwidth requirements/allocations, as shown in **FIG. 3**. Initially, each device determines its average bandwidth requirements in each of the above-mentioned priority classes (step **60**). These requirements are then compared against the current bandwidth allocations (step **62**) and a determination is made as to whether the current allocations are adequate, include excess bandwidth or provide for insufficient bandwidth (step **64**). If the current allocations are adequate, no further action is needed, and the device repeats the bandwidth assessment periodically (step **66**). If the current allocations are more than what is needed, the device may release excess bandwidth (step **68**) by informing the network master of the situation and requesting a new, reduced bandwidth allocation. If, however, the current allocations are insufficient, the device transmits a request for additional bandwidth to the master (step **70**).

[0037] As for the network master, the dynamic bandwidth allocations and requests are managed as shown in **FIG. 4**. The bandwidth reports (e.g., requests for new allocations) are received from the network devices (including the master's own reports) (step **80**) and compared against the current utilization scheme, after taking into account any bandwidth being released (step **82**). The result of this comparison is checked to determine whether any excess bandwidth remains (step **84**). If not, the requests for additional bandwidth are rejected (step **86**).

[0038] If, however, additional bandwidth is available in the subnet, the requests for new bandwidth to accommodate isochronous streams are satisfied up to the total available bandwidth (step **88**). If all of these requests are satisfied (or if there are none), a check is made to see if any additional bandwidth is available (step **90**) and, if so, the remaining requests are satisfied in the order discussed above (step **92**). Of course, if no bandwidth is available, or at the point it is exhausted, any remaining requests are rejected. This process may be repeated periodically as new bandwidth reports are received and analyzed.

[0039] Although not shown in detail in the figure, it should be appreciated that the bandwidth reports could be received in response to a request by the master therefor. For example, if the master device needs to accommodate a high priority stream from a device, the master could request bandwidth reports to determine which device(s) has/have available bandwidth that could be released to accommodate the high priority stream. With such information (which could even indicate that the device with the high priority stream has other bandwidth, e.g., associated with another (low priority) stream that could be released) the master can begin negotiations to free up bandwidth to accommodate the high priority stream.

[0040] Thus, a scheme for dynamically allocating bandwidth within a computer network communication channel has been described. Although discussed with reference to certain illustrated embodiments, the present invention should not be limited thereby. Instead, the present invention should only be measured in terms of the claims that follow.

What is claimed is:

1. A method, comprising dynamically allocating bandwidth within a communication channel of a computer network according to bandwidth requests of devices within the computer network.

2. The method of claim 1 wherein the bandwidth requests include releases of excess bandwidth.

3. The method of claim 2 wherein the communication channel comprises a spread spectrum communication channel.

4. The method of claim 3 wherein the communication channel further comprises a wireless communication channel.

5. The method of claim 1 wherein the bandwidth is dynamically allocated according to priorities of the requests.

6. The method of claim 5 wherein the priorities of the requests are arranged such that bandwidth requests associated with isochronous transmissions within the computer network are accorded highest priority.

7. The method of claim 1 wherein the bandwidth requests are made at any times during which the devices have active connections within the computer network.

8. The method of claim 1 wherein dynamically allocating bandwidth comprises renegotiating bandwidth for a low priority stream associated with one of the devices to accommodate a high priority stream associated with the same or another of the devices.

9. A method, comprising maintaining a table of bandwidth allocations for devices of a computer network so as to account for bandwidth utilization within the network.

10. The method of claim 9 wherein the table is maintained by a master device within the network.

11. The method of claim 10 wherein table includes bandwidth allocations for information streams having varying priorities.

12. The method of claim 11 wherein isochronous streams are accorded highest priority within the network.

13. The method of claim 12 wherein the table is dynamically updated according to bandwidth requests by the devices within the network and allocations made in accordance therewith.

14. The method of claim 13 wherein the bandwidth requests include requests for additional bandwidth and releases of excess bandwidth.

15. The method of claim 14 wherein bandwidth requests associated with other than isochronous streams are satisfied according to a process wherein those of the requests associated with the device having the lowest overall bandwidth utilization are satisfied first, followed by remaining requests.

16. The method of claim 15 wherein the remaining requests are satisfied in an order according to the priorities of the streams associated therewith and on a first-come-first-serve basis thereafter.

* * * * *

39/3,K/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016319216 **Image available**
WPI Acc No: 2004-477111/200445
XRPX Acc No: N04-375847
Universal serial bus device **interface controller, has first in-first out** partition **configurations** dynamically **change from** ping **-pong first in-first out for isochronous data and circular first in-first out for non-isochronous data**
Patent Assignee: CYPRESS SEMICONDUCTOR CORP (CYPR-N)
Inventor: LUKE D; PEW F; PROVENCIO K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6745264	B1	20040601	US 2002196106	A	20020715	200445	B

Priority Applications (No Type Date): US 2002196106 A 20020715
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6745264	B1		13	G06F-009/445	

Universal serial bus device **interface controller, has first in-first out** partition **configurations** dynamically **change from** ping **-pong first in-first out for isochronous data and circular first in-first out for...**

Abstract (Basic):
... The controller (72) has a DMA **interface** controller (82) to configure logic units in the controller **according** to selected configuration parameters. The logic units include a memory (16) configurable into multiple first in-first out (FIFO) regions with different configurations. The configurations **dynamically** change from a **ping** -pong FIFO for an isochronous data and a circular FIFO for a non-isochronous data.
... INDEPENDENT CLAIM is also included for a method for configuring a memory for universal serial **bus** communication...

...Used in a universal serial **bus device** .
...

...The FIFO **partition** configurations **dynamically** change from the **ping** -pong FIFO for isochronous data and the single circular FIFO for other types of data...

...associated with differences in data rates between the read and write side of the memory **partition** and making it easy to keep **track** of **data** associated with each frame...
...The drawing shows a block diagram of an **interface** controller...

...Universal serial **bus device** interface controller (72...

... **Device** processor (74...

...DMA **interface** controller (82
...Title Terms: **BUS** ;
International Patent Class (Main): **G06F-009/445**

International Patent Class (Additional): **G06F-013/00** ...

... **G06F-013/14** ...

... **G06F-013/40**
Manual Codes (EPI/S-X): **T01-C07C** ...

... **T01-H05B2** ...

... **T01-H07A**

42/3,K/25 (Item 25 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010992897 **Image available**
WPI Acc No: 1996-489846/199649
XRPX Acc No: N96-412778
Printing device **e.g. page printer, copier, matrix printer - has** number **of data buffer** assigned **to ports, in which** size **of buffer is made arbitrarily changeable**
Patent Assignee: RICOH KK (RICO)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8249142	A	19960927	JP 9578290	A	19950309	199649	B

Priority Applications (No Type Date): JP 9578290 A 19950309
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8249142	A		8	G06F-003/12	

Printing device **e.g. page printer, copier, matrix printer...**

...**has** number **of data buffer** assigned **to ports, in which** size **of buffer is made arbitrarily changeable**
...Abstract (Basic): The **device** forms a variable image on paper using data sent from a host, under the control of an image controller. Data is received from the host through many **ports** . **Data** buffers are **assigned** at each **port** . A **data** controller stores the **amount** of data sent to the port and frequency of data usage...

...Printing is performed **according** to the image processed by the image controller. The **size** of the data buffer is **assigned** to the part is made **changeable** .
...

...ADVANTAGE - Enables suitable setting of buffer **size** . Shortens data transfer time. Raises **amount** of buffers in areas of HF of utilization. Enables effective usage of resources. Enables efficient
...Title Terms: **DEVICE** ;
International Patent Class (Main): **G06F-003/12**
Manual Codes (EPI/S-X): **T01-C05A**

42/3,K/37 (Item 37 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007674773 **Image available**
WPI Acc No: 1988-308705/198844
XRPX Acc No: N88-234318
Network communications adaptor with partitioned **common buffer memory - has node control logic** allocating **available bandwidth and** connecting **alternate memory banks cyclically to common** bus
Patent Assignee: NETWORK SYSTEMS CORP (NETW-N); NETWORK SYST CORP (NETW-N)
Inventor: HUGHES J P; HUMPHREY D J; PETERSON W A; ROIGER W R
Number of Countries: 007 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 288636	A	19881102	EP 87308161	A	19870916	198844	B
US 4933846	A	19900612	US 8741985	A	19870424	199031	
CA 1289673	C	19910924				199144	
EP 288636	B1	19940216	EP 87308161	A	19870916	199407	
DE 3789104	G	19940324	DE 3789104	A	19870916	199413	
			EP 87308161	A	19870916		

Priority Applications (No Type Date): US 8741985 A 19870424
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 288636	A	E	55		
Designated States (Regional): DE FR GB IT NL					
EP 288636	B1	E	55	G06F-015/16	
Designated States (Regional): DE FR GB IT NL					
DE 3789104	G			G06F-015/16	Based on patent EP 288636

Network communications adaptor with partitioned **common buffer memory**...

...**has node control logic** allocating **available bandwidth and** connecting **alternate memory banks cyclically to common** bus

...Abstract (Basic): is organised into two interleaved banks which operate independently and concurrently under the control of **bus** switching logic with separate address, control and data buses. The dual 16-bit architecture efficiently **couples** the central memory (100) to a mixture of 32-bit microprocessors (100,112) and 16...

...A dedicated microprocessor **routes** message traffic through the adaptor, and manages **dynamic** page-by-page **assignment** of central memory space. Node control logic (130) broadcasts the identification of a particular processor...
...Abstract (Equivalent): memory means (100) for storing data at addressable locations, said buffer memory means (100) being **partitioned** into first and second independently and concurrently operating interleaved banks (0, 1); (b) first and second common **bus** means (102, 104) selectively **connectable** on an alternating basis to said first and second banks for providing, on a time...

...representing signals therein, characterised in that the first and second common buses (102, 104) are **connected** to said first and second banks (0, 1) on an alternating basis; and in that the adaptor further comprises; (c) first and second read data **bus** means (106, 108)

selectively **connectable** on an alternating basis to said two banks (0, 1) for carrying data representing signals...

...memory means (100); (d) a plurality of processing means (110, 112, 114, 116, 118) individually **coupled** to said first and second command buses (102, 104) and read data buses (106, 108...

...of processing means having input-output means (120, 124, 126, 128) for communication with digital **devices** **connected** thereto; and (e) node control means (130) including memory access control means (202) for **synchronously** and cyclicly **connecting** alternate ones of said first and second banks (0, 1) to said first and second common **bus** means (102, 140) and said first and second read data **bus** means (106, 108) and further including storage protection logic (204, 206) individually associated with each...

...processing means (110, 112, 114, 116, 118), and present on said first and second common **bus** means (102, 104) to a predetermined key I. **assigned** to said one of said plurality of processing means (110, 112, 114. 116, 118) for...

...Abstract (Equivalent): memory is configured into two banks, each bank operating independently and concurrently under control of **bus** switching logic with separate address, control and data buses...

...The **bus** switching logic **allocates** all of the available bandwidth to the individual processors **coupled** to the buses based upon a predetermined profile established at the time of system **installation** . One of the interconnected processors is **designated** as the node controller and it includes circuitry and software for implementing inter processor interrupt...

...Title Terms: **PARTITION** ;

International Patent Class (Main): **G06F-015/16**

International Patent Class (Additional): **G06F-012/14** ...

... **G06F-013/16** ...

... **G06F-013/26**

Manual Codes (EPI/S-X): **T01-H05B** ...

... **T01-J02** ...

... **T01-J02A**